Q3

module dec2to4 (input[1:0] i, input en, output [3:0] d);

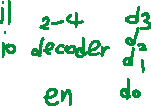
wire inva,invb;

not a (i0', i0);

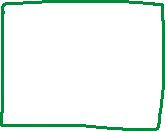
not b (i1', i1);



and s(d0, i0', i1', en);



and t (d1, i1', i0, en);



and u (d2, i0’, i1, en);



and v (d3, i0, i1, en);



endmodule



**module dec2to4 (input [1:0] a , input enable,**

**output [3:0] one-hot);**

**wire [1:0] a;**

**wire enable;**

**wire [3:0] one-hot;**

**assign one-hot[0] = ~a[1]&& ~a[0] &&**

**enable;**

**assign one-hot[1] = ~a[1]&& a[0] &&**

**enable;**

**assign one-hot[2] = a[1]&& ~a[0] &&**

**enable;**

**assign one-hot[3] = a[1]&& a[0] &&**

**enable;**

**endmodule**

**module queuecont (input [1:0] sel,**

**input full,**

**output [3:0] queue,**

**output stop);**

**dec2to4 (.a(sel),.enable(~full),.one-hot(queue));**

**endmodule**

Q4



Assign output x = a | ~c |d | e ;



Assign output y = a & b & ~e ;

